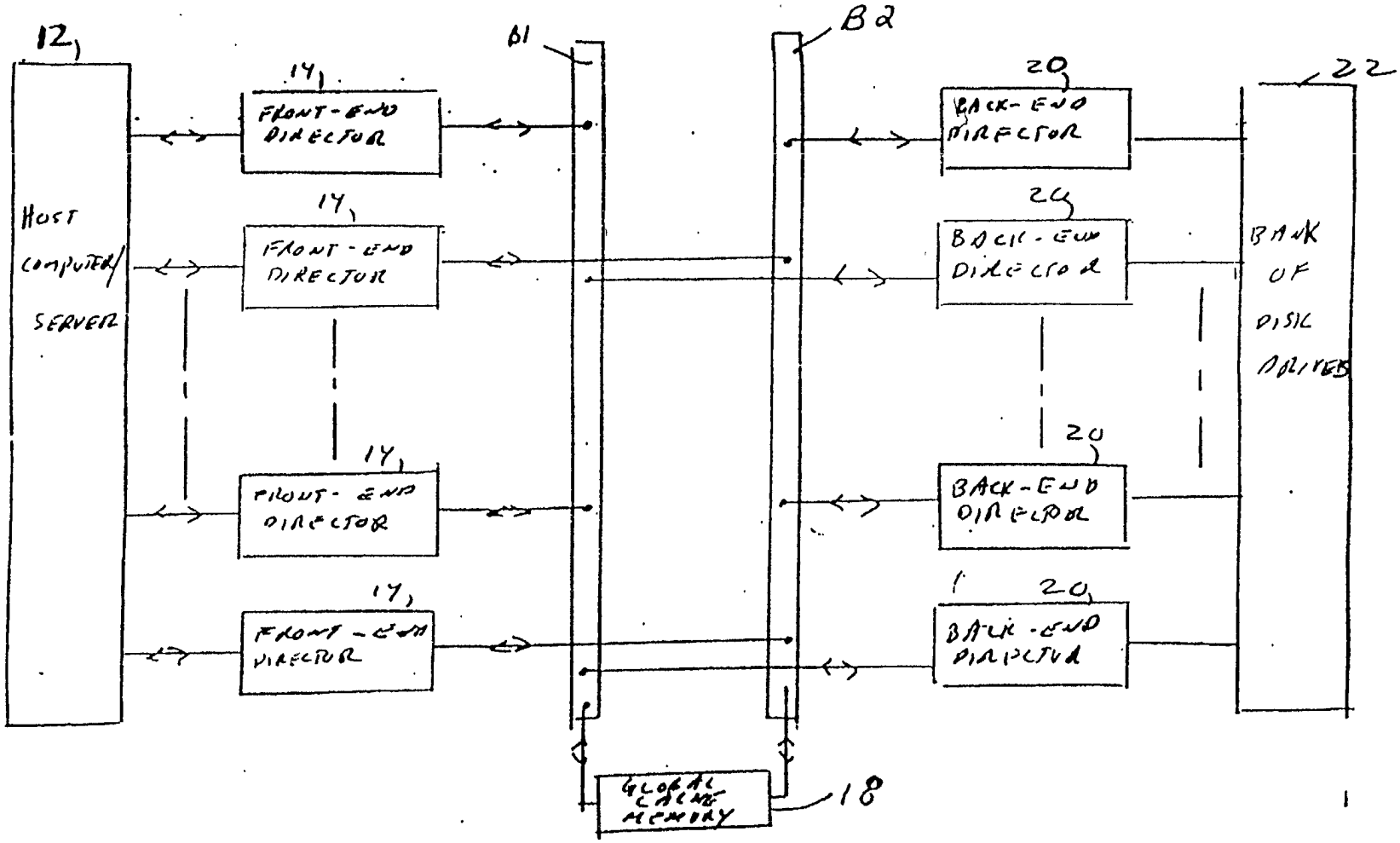
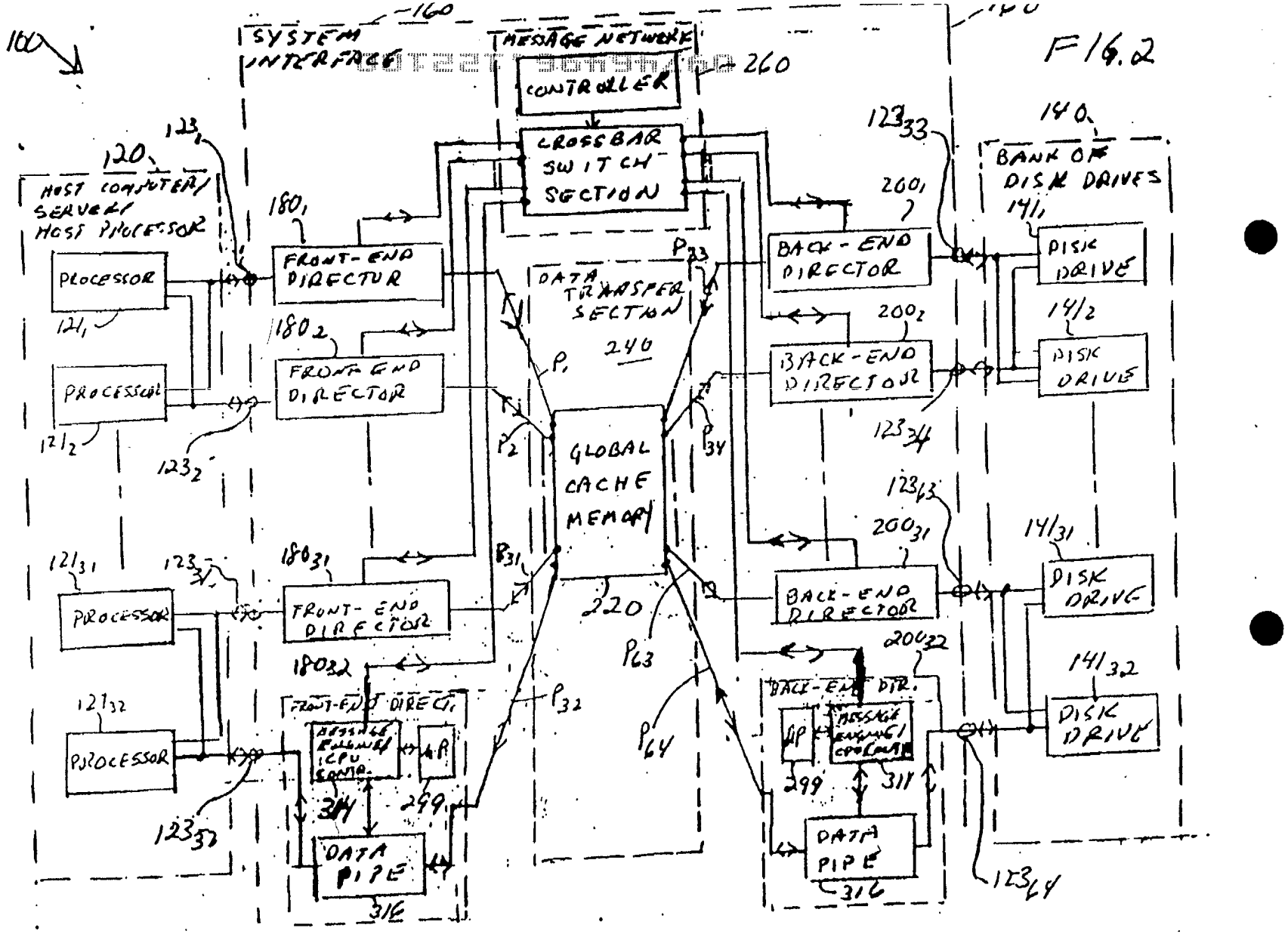
DOT22F 96h9h260

FIG. 1
PRIOR ART




100
SYSTEM INTERFACE
160
MESSAGE NETWORK
CONTROLLER
260
CROSSBAR SWITCH SECTION
120
HOST COMPUTER/ SERVER/ HOST PROCESSOR
PROCESSOR
PROCESSOR
PROCESSOR
PROCESSOR
FRONT-END DIRECTOR
FRONT-END DIRECTOR
FRONT-END DIRECTOR
DATA TRANSFER SECTION
240
GLOBAL CACHE MEMORY
220
BACK-END DIRECTOR
BACK-END DIRECTOR
BACK-END DIRECTOR
DATA PIPE
316
BANK OF DISK DRIVES
140
DISK DRIVE
DISK DRIVE
DISK DRIVE
DISK DRIVE

F16.2

16 64
x4

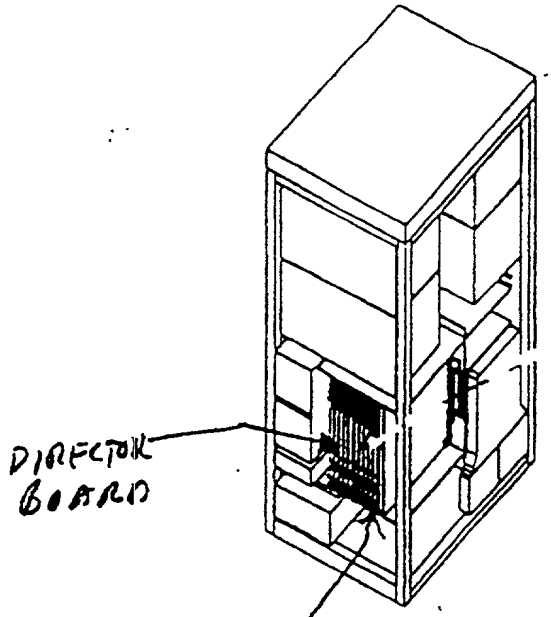
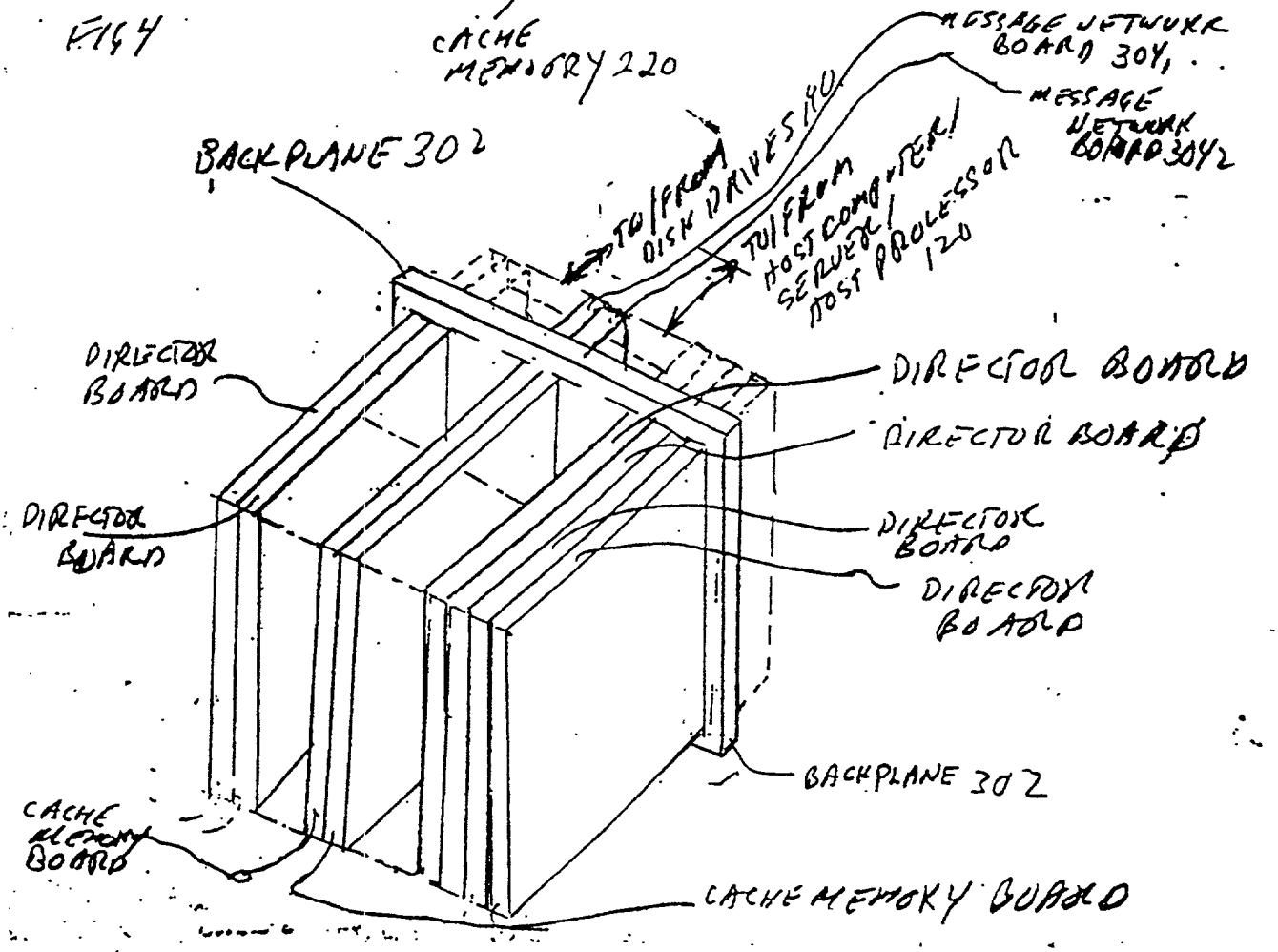

DIRECTOR BOARD
CACHE MEMORY 220

FIG. 3

FIG 4


MESSAGE NETWORK BOARD 304,
MESSAGE NETWORK BOARD 304₂
BACKPLANE 302
TO/FROM DISK DRIVES 140
TO/FROM HOST COMPUTER/ HOST PROCESSOR 120
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
BACKPLANE 302
CACHE MEMORY BOARD
CACHE MEMORY BOARD

DOT227 96h9h260

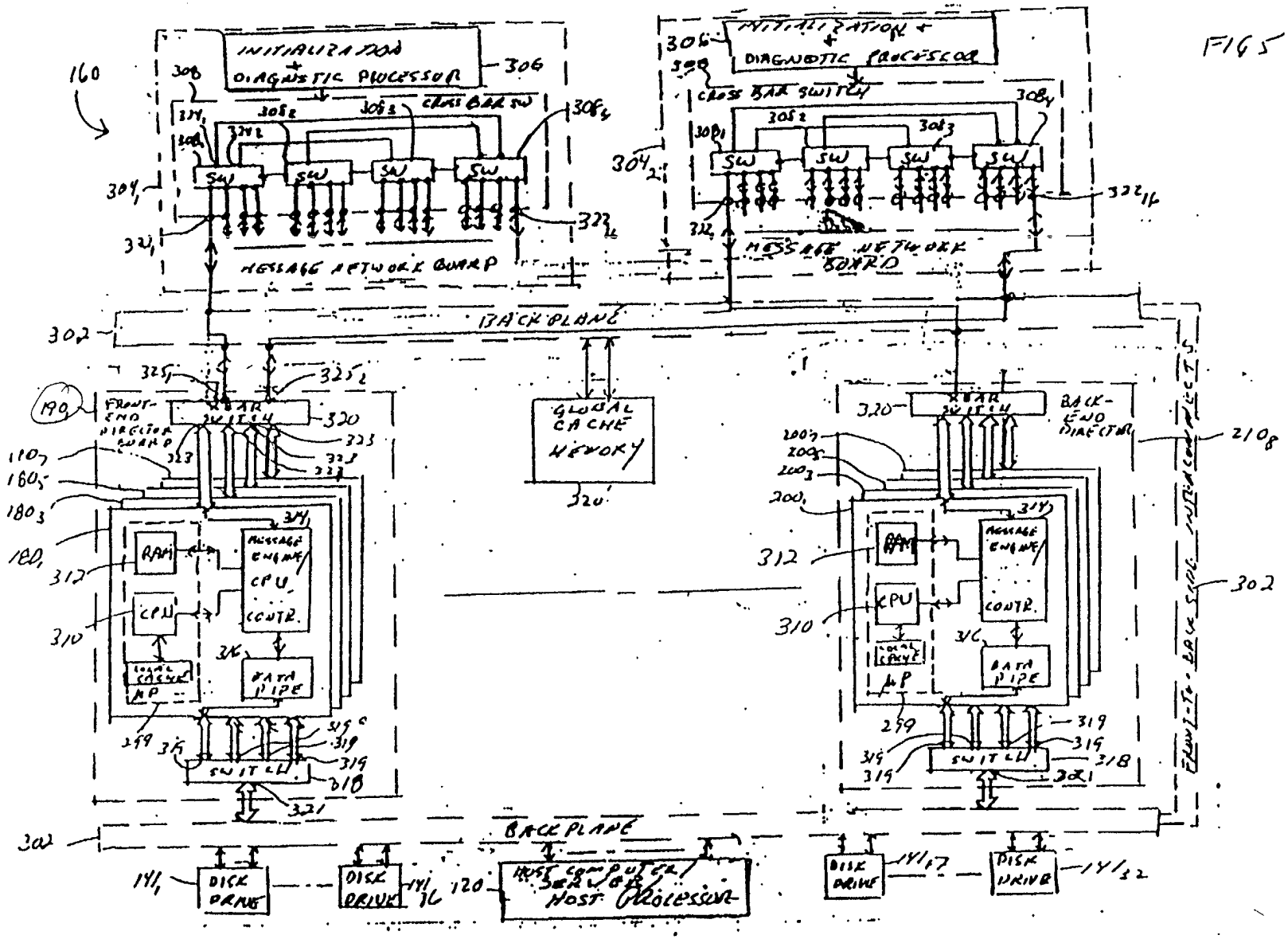


FIG 5

DOT22T "96h9h260

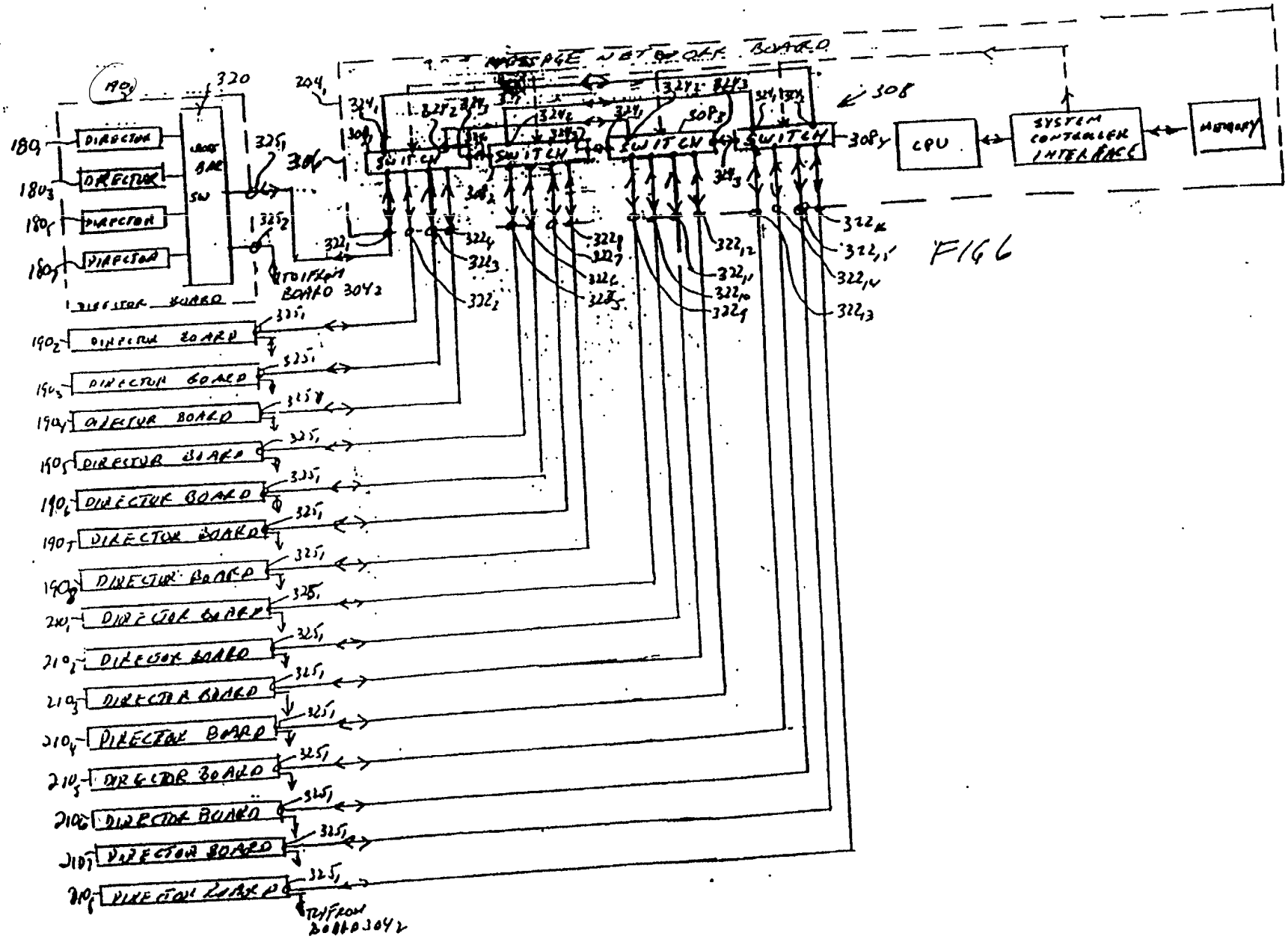
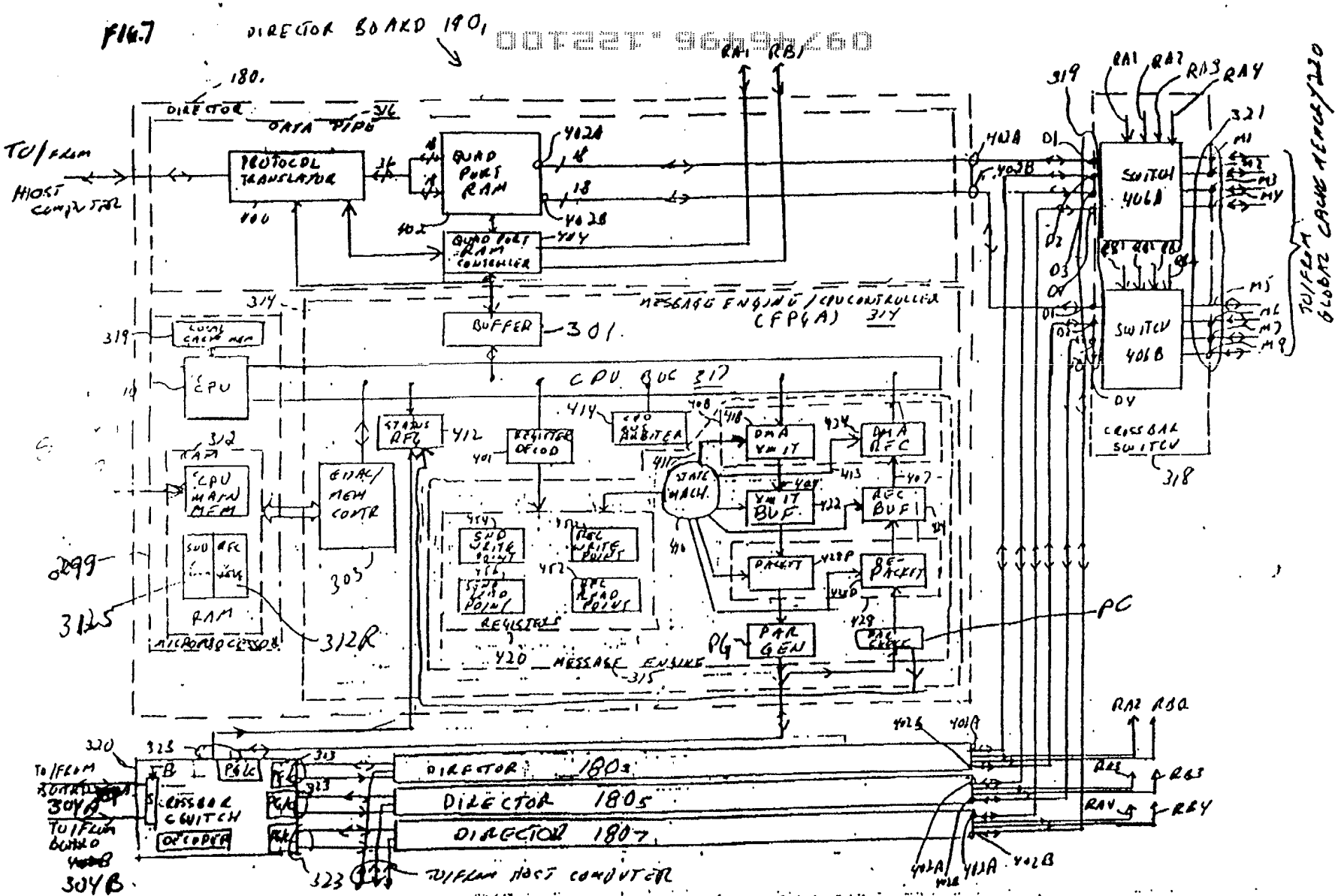
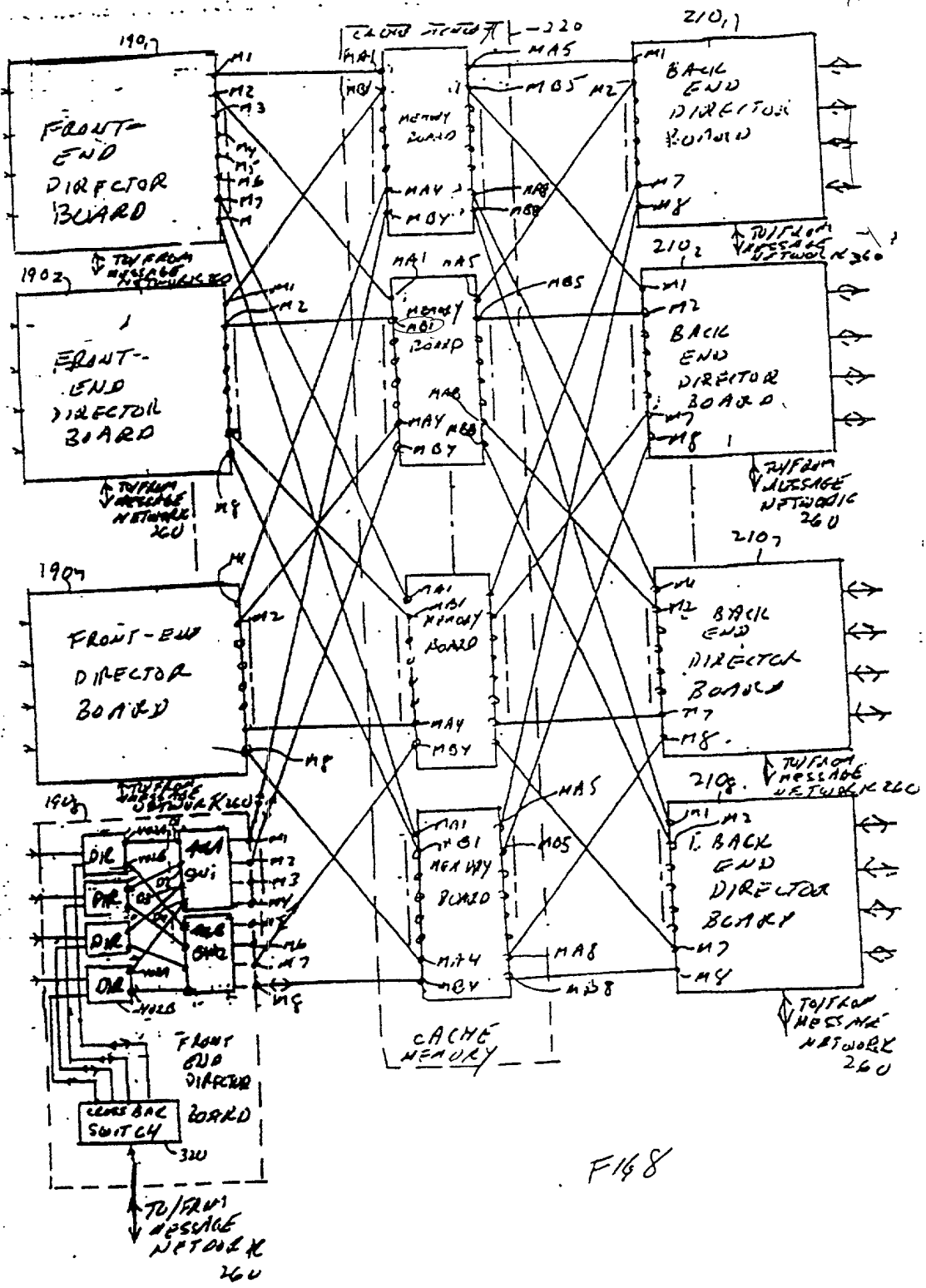


FIG 6

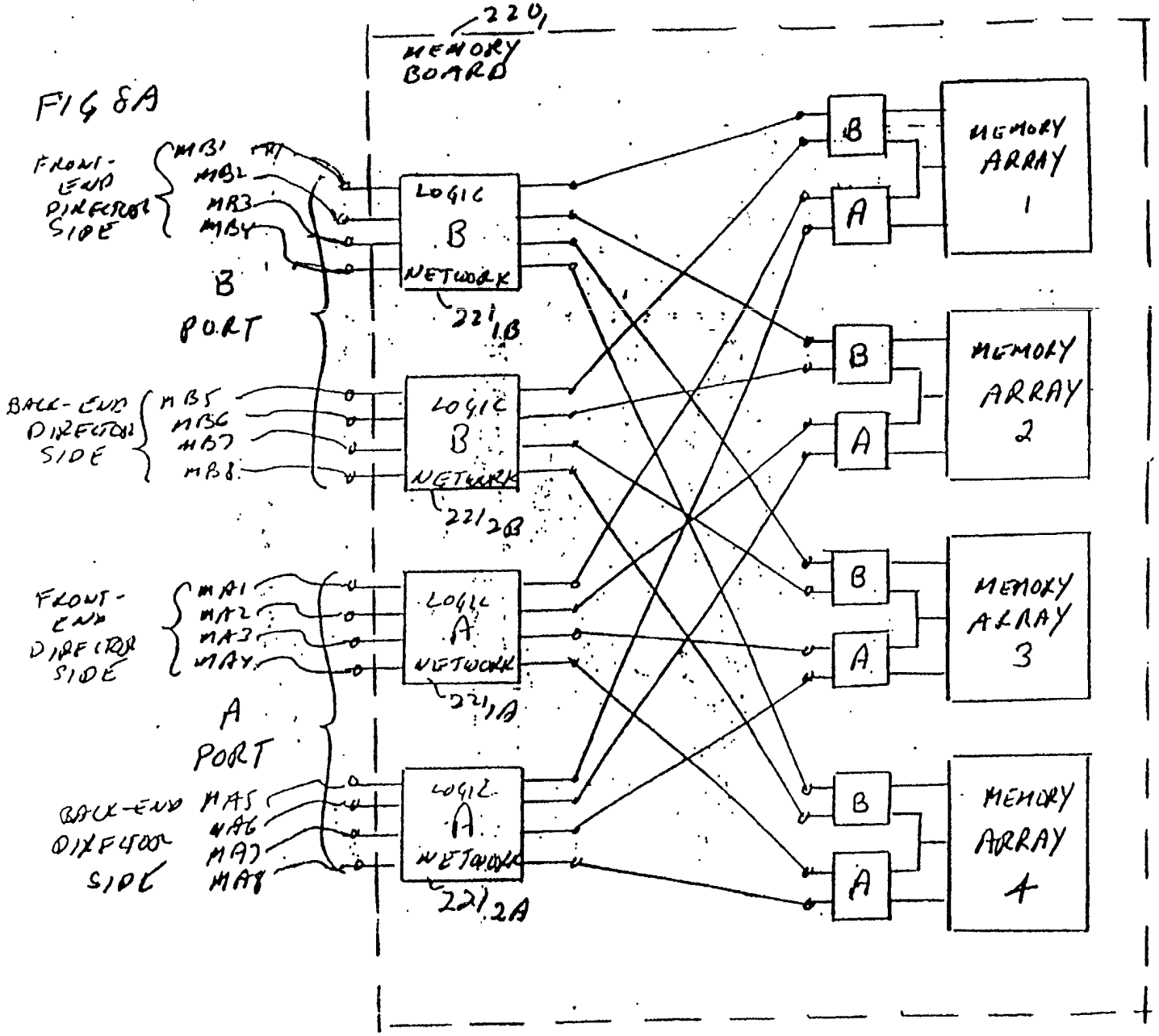
FIG.7


DIRECTOR BOARD 190
180
DIRECTOR
DATA PIPE
TO/FROM HOST COMPUTER
PROTOCOL TRANSLATOR
QUAD PORT RAM
QUAD PORT RAM CONTROLLER
BUFFER
MESSAGE ENGINE / CPU CONTROLLER (CPPA)
CPU BUS
CPU
CPU MAIN MEM
RAM
MICROPROCESSOR
EDAC / MEM CONTR
STATUS REG
REGISTER DECOD
BUS ARBITER
STATE MACH.
DMA XMIT
DMA REC
XMIT BUF
REC BUF
PACKIT
DE-PACKIT
PAR GEN
PAR CHECK
REGISTERS
MESSAGE ENGINE
SND WRITE POINT
REC WRITE POINT
SND READ POINT
REC READ POINT
CROSSBAR SWITCH
SWITCH 406A
SWITCH 406B
CROSSBAR SWITCH
TO/FROM GLOBAL CACHE MEMORY 220
DIRECTOR 180B
DIRECTOR 180C
DIRECTOR 180D
TO/FROM HOST COMPUTER
TO/FROM CONTROL BUS 304A
TO/FROM CONTROL BUS 304B
CROSSBAR SWITCH
DECODER
PC


FRONT-END DIRECTOR BOARD
FRONT-END DIRECTOR BOARD
FRONT-END DIRECTOR BOARD
FRONT END DIRECTOR BOARD
CACHE MEMORY
MEMORY BOARD
BACK END DIRECTOR BOARD
BACK END DIRECTOR BOARD
BACK END DIRECTOR BOARD
BACK END DIRECTOR BOARD
CROSS BAR SWITCH
TO/FROM MESSAGE NETWORK 260

F16 8

DOT22T: 96h9Hr60



00722F "96h9h260

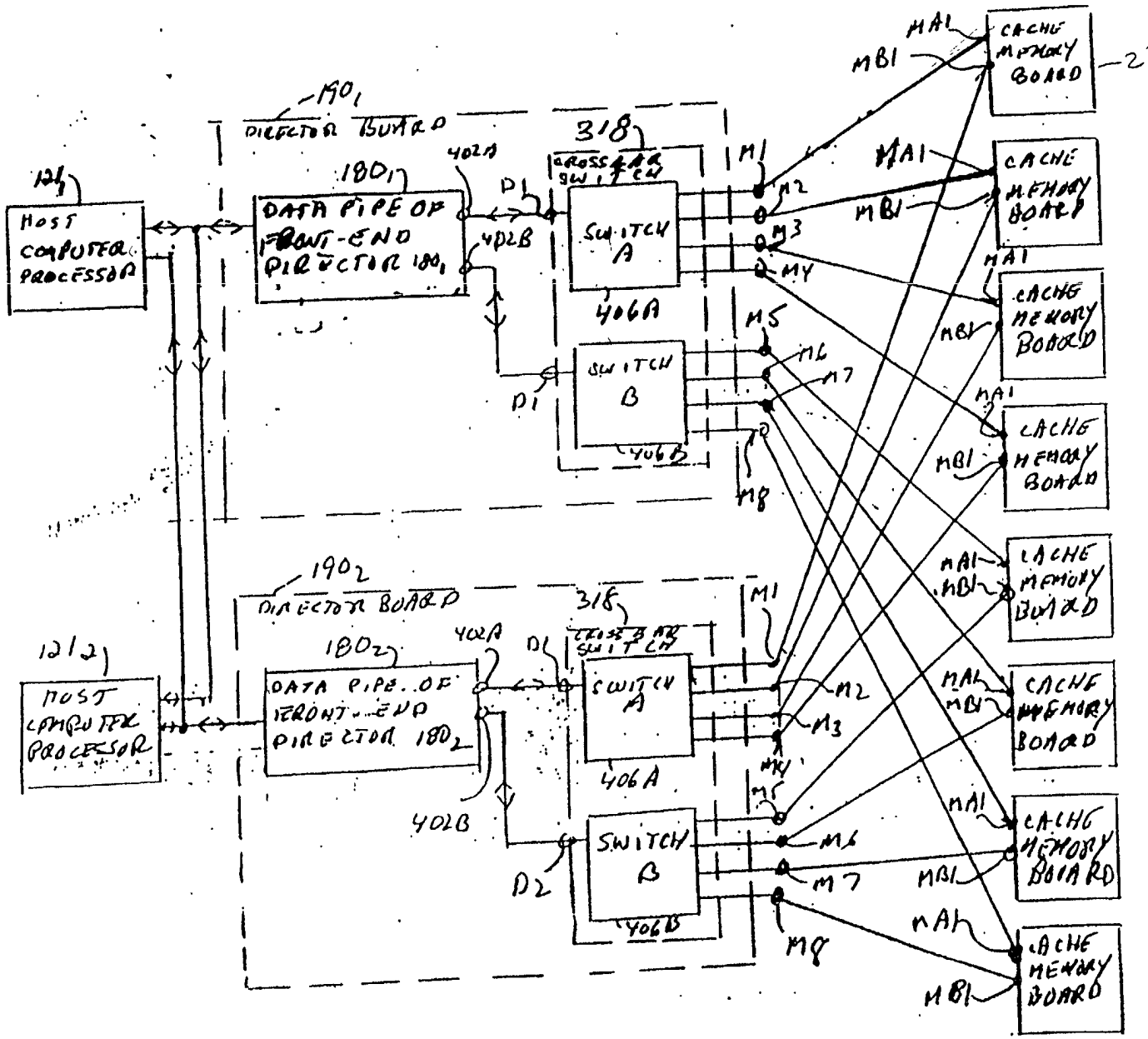


FIG 8B

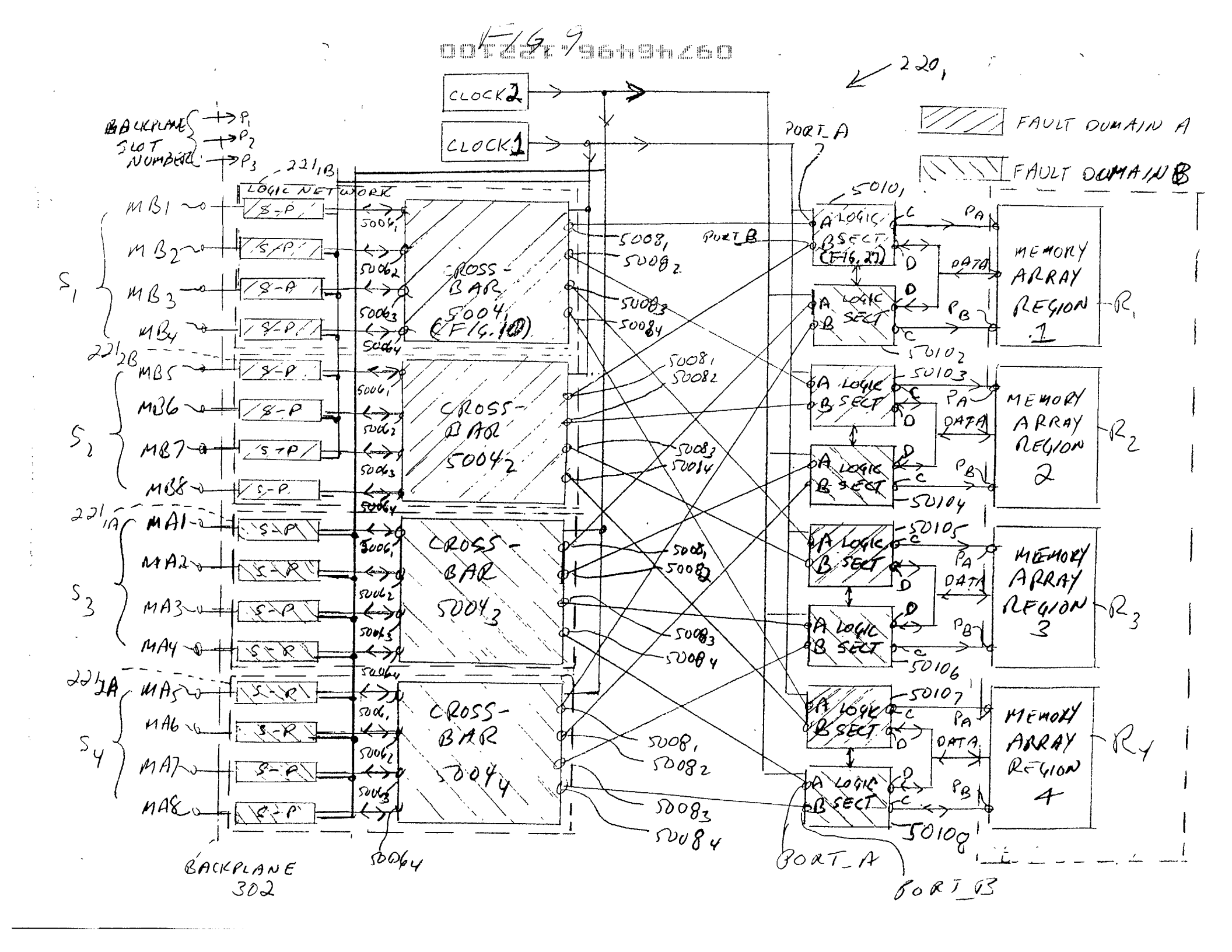
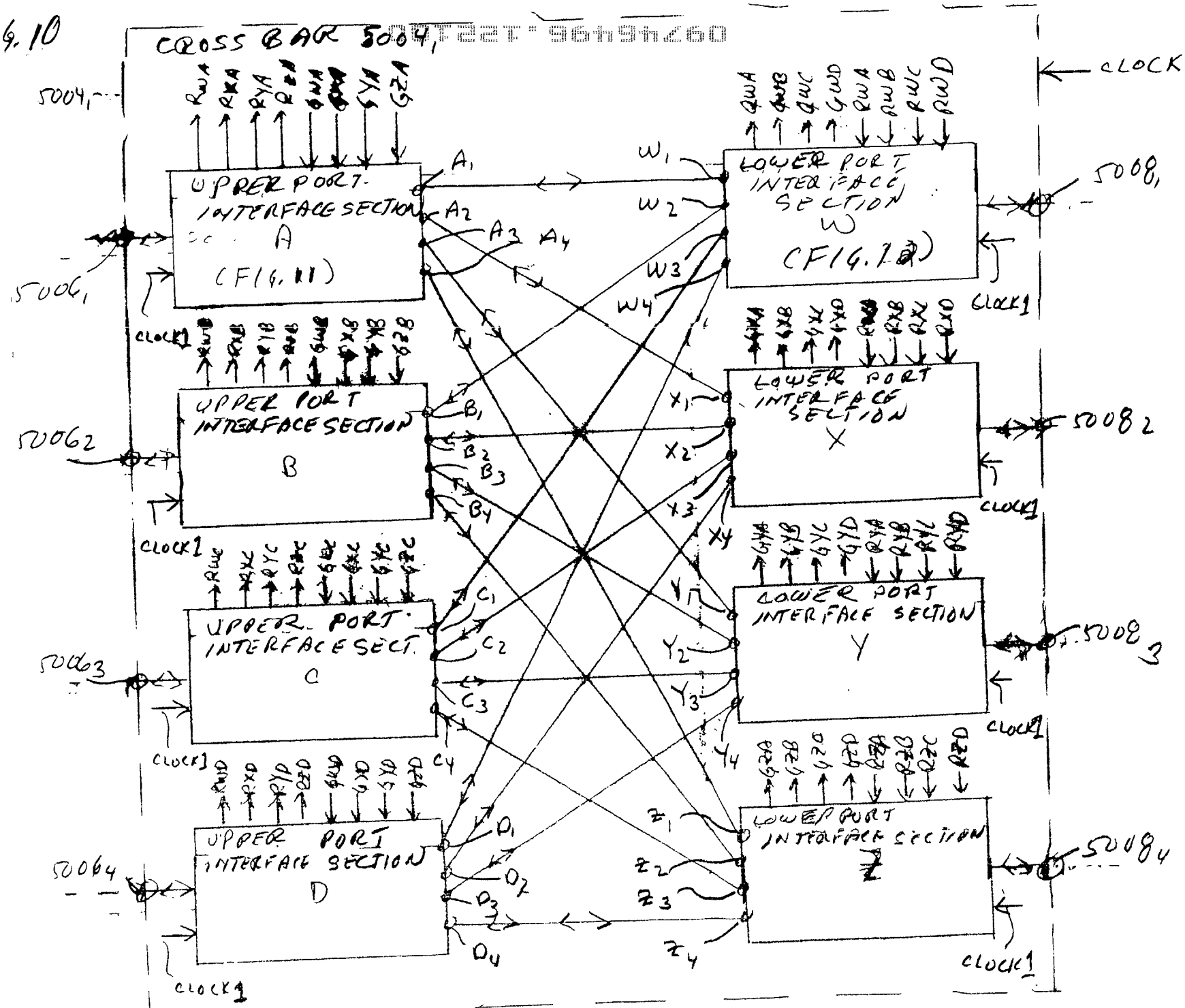


FIG. 9
220₁
CLOCK 2
CLOCK 1
BACKPLANE SLOT NUMBER
P1
P2
P3
221₁B
LOGIC NETWORK
MB1
MB2
MB3
MB4
S1
221₂B
MB5
MB6
MB7
MB8
S2
221₁A
MA1
MA2
MA3
MA4
S3
221₂A
MA5
MA6
MA7
MA8
S4
S-P
5006₁
5006₂
5006₃
5006₄
CROSS-BAR 5004 (FIG. 10)
CROSS-BAR 5004₂
CROSS-BAR 5004₃
CROSS-BAR 5004₄
5008₁
5008₂
5008₃
5008₄
PORT_B
PORT_A
5010₁
A LOGIC B SECT (FIG. 27)
5010₂
5010₃
5010₄
5010₅
5010₆
5010₇
5010₈
C
D
DATA
PA
PB
MEMORY ARRAY REGION 1
MEMORY ARRAY REGION 2
MEMORY ARRAY REGION 3
MEMORY ARRAY REGION 4
R1
R2
R3
R4
FAULT DOMAIN A
FAULT DOMAIN B
BACKPLANE 302
5006₄
PORT_A
PORT_B

FIG. 10


CROSS BAR 5004
UPPER PORT INTERFACE SECTION A (FIG. 11)
UPPER PORT INTERFACE SECTION B
UPPER PORT INTERFACE SECTION C
UPPER PORT INTERFACE SECTION D
LOWER PORT INTERFACE SECTION W (FIG. 12)
LOWER PORT INTERFACE SECTION X
LOWER PORT INTERFACE SECTION Y
LOWER PORT INTERFACE SECTION Z
CLOCK 1
5004
5006
5008

DOT22T* 96h9h760

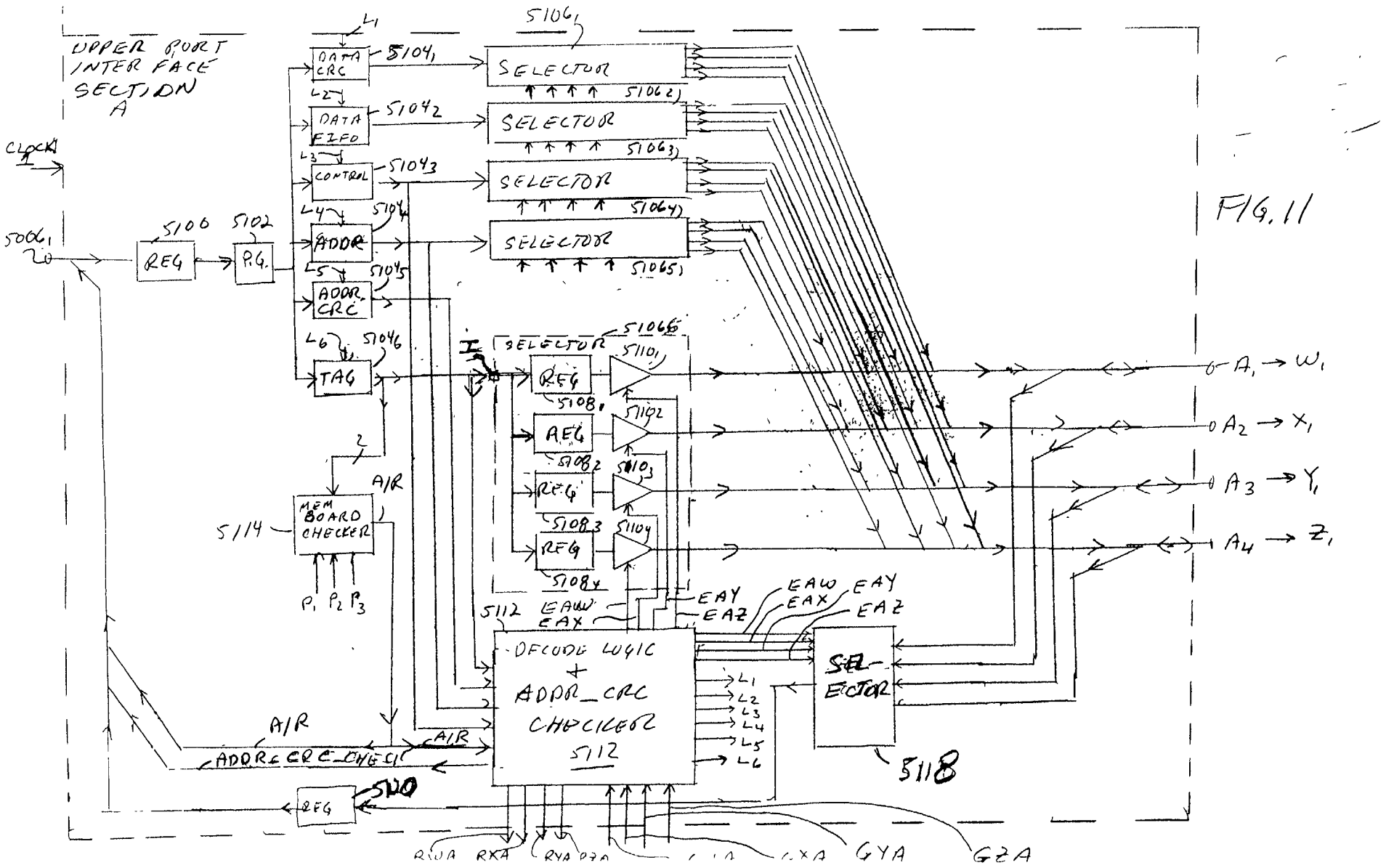


FIG. 11

FIG. 12

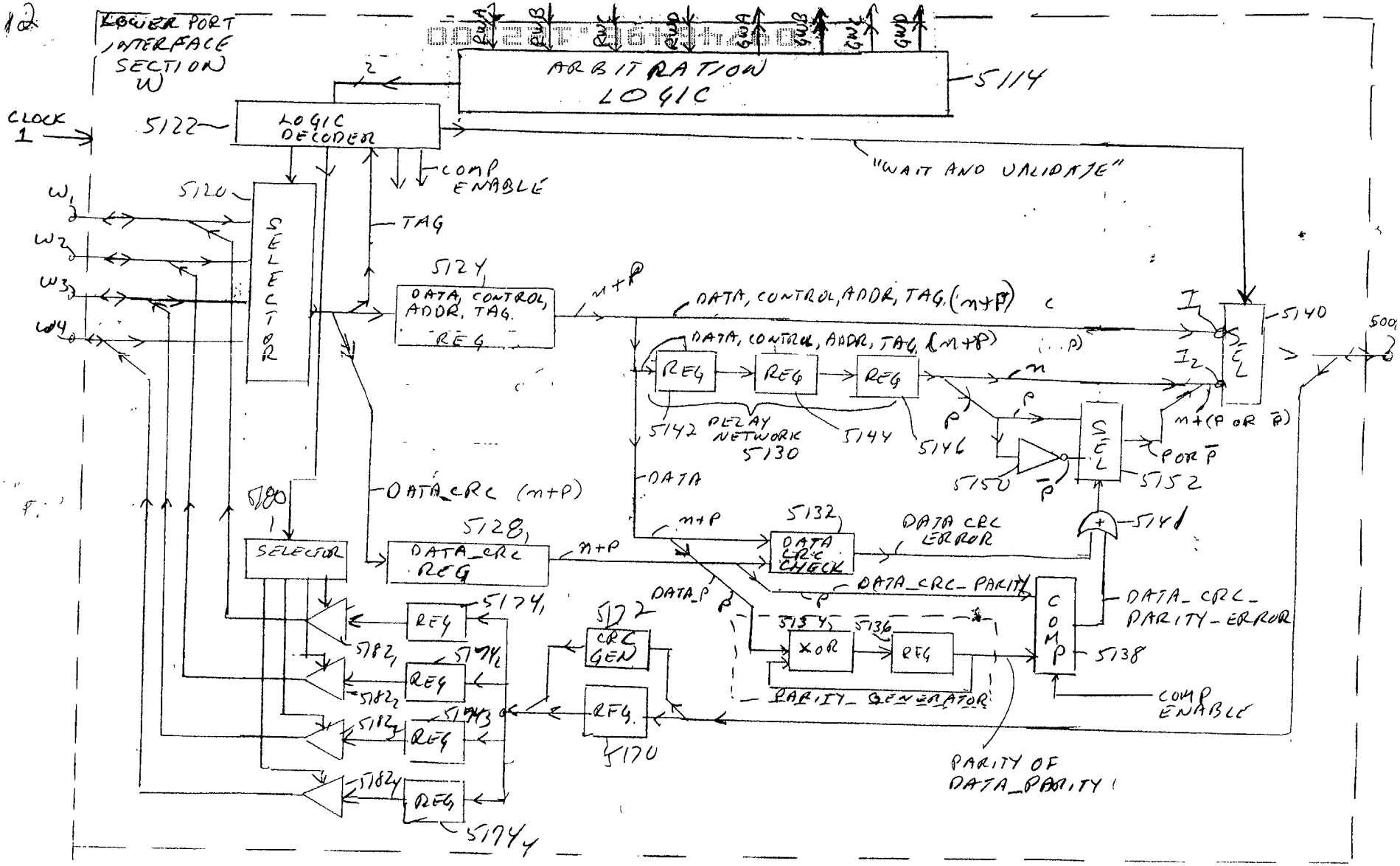
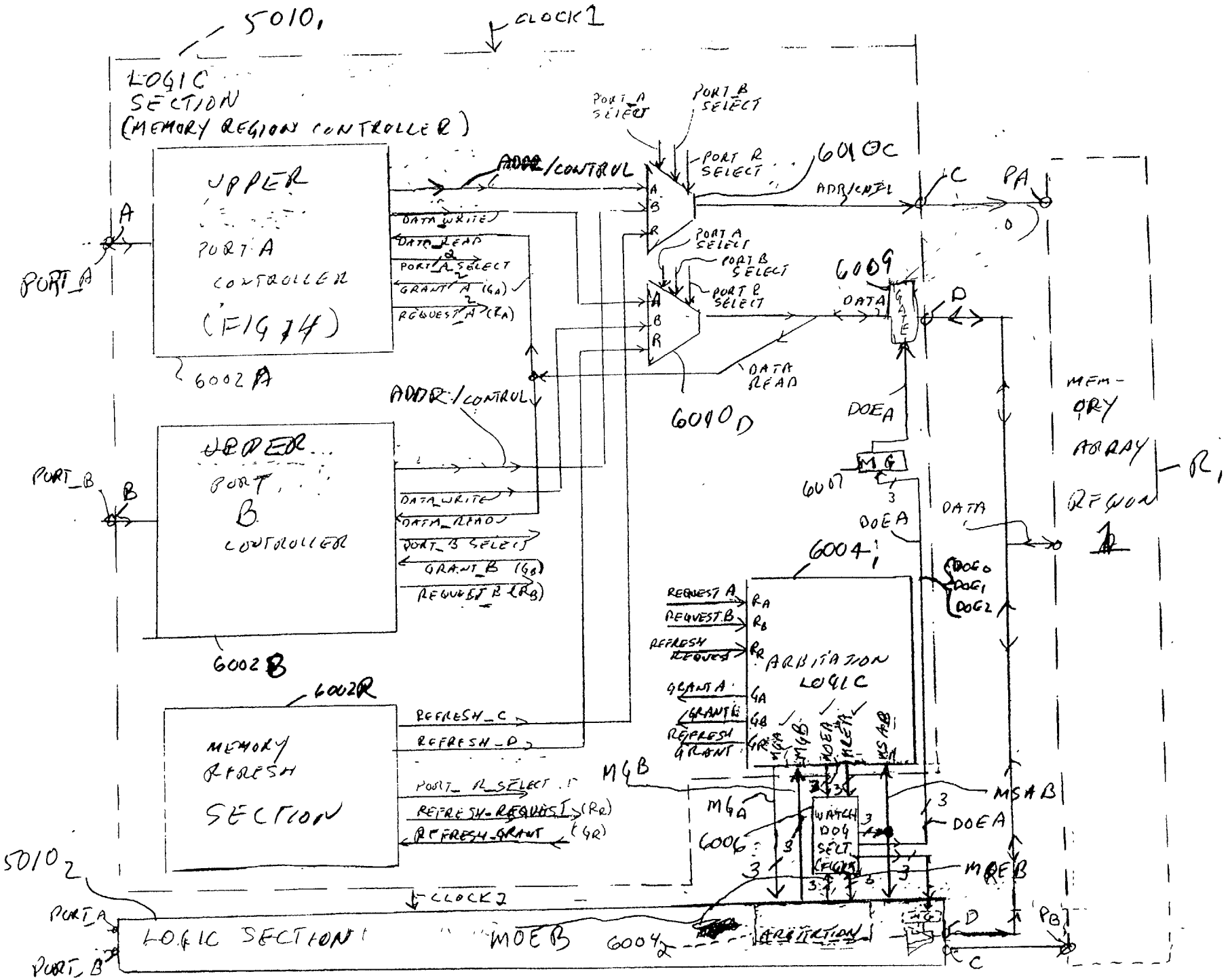

LOWER PORT INTERFACE SECTION W
ARBITRATION LOGIC
5114
CLOCK 1
5122
LOGIC DECODER
COMP ENABLE
"WAIT AND VALIDATE"
W1
W2
W3
W4
5120
SELECTOR
TAG
5124
DATA, CONTROL, ADDR, TAG. REG
DATA, CONTROL, ADDR, TAG. (m+P)
REG
REG
REG
5142 DELAY NETWORK 5130
5144
5146
5150
5140
SEL
I1
I2
m+(P OR P̄)
P OR P̄
5152
5148
5500
DATA
DATA_CRC (m+P)
5180
SELECTOR
5128
DATA_CRC REG
m+P
5132
DATA CRC CHECK
DATA CRC ERROR
DATA_CRC_PARITY
DATA_CRC_PARITY_ERROR
DATA_P
5174
REG
5182
5172
CRC GEN
5154
XOR
5156
REG
COMP
5138
PARITY_GENERATOR
COMP ENABLE
5170
PARITY OF DATA_PARITY

FIG. 13


5010,
CLOCK 1
LOGIC SECTION (MEMORY REGION CONTROLLER)
UPPER PORT A CONTROLLER (FIG 14)
6002A
PORT_A
A
ADDR/CONTROL
DATA_WRITE
DATA_READ
PORT_A SELECT
GRANT_A (GA)
REQUEST_A (RA)
PORT A SELECT
PORT B SELECT
PORT R SELECT
6010C
ADDR/CNTL
C
PA
A
B
R
6009
DATA
GATE
D
DATA READ
6010D
DOEA
MG
6007
3
MEM-ORY ARRAY REGION 1
R1
UPPER PORT B CONTROLLER
6002B
PORT_B
B
DATA_WRITE
DATA_READ
PORT_B SELECT
GRANT_B (GB)
REQUEST_B (RB)
6004,
REQUEST A
REQUEST B
REFRESH REQUEST
GRANT A
GRANT B
REFRESH GRANT
RA
RB
RR
GA
GB
GR
ARBITRATION LOGIC
DOG0
DOG1
DOG2
MGA
MGB
DOEA
MSAB
6002R
MEMORY REFRESH SECTION
REFRESH_C
REFRESH_D
PORT_R_SELECT
REFRESH_REQUEST (RR)
REFRESH_GRANT (GR)
MGB
MGA
MSAB
DOEA
6006
WATCH DOG SELECT REGISTER
MREB
5010 2
CLOCK 2
PORT_A
PORT_B
LOGIC SECTION
MOEB
6004 2
ARBITRATION
D
PB
C

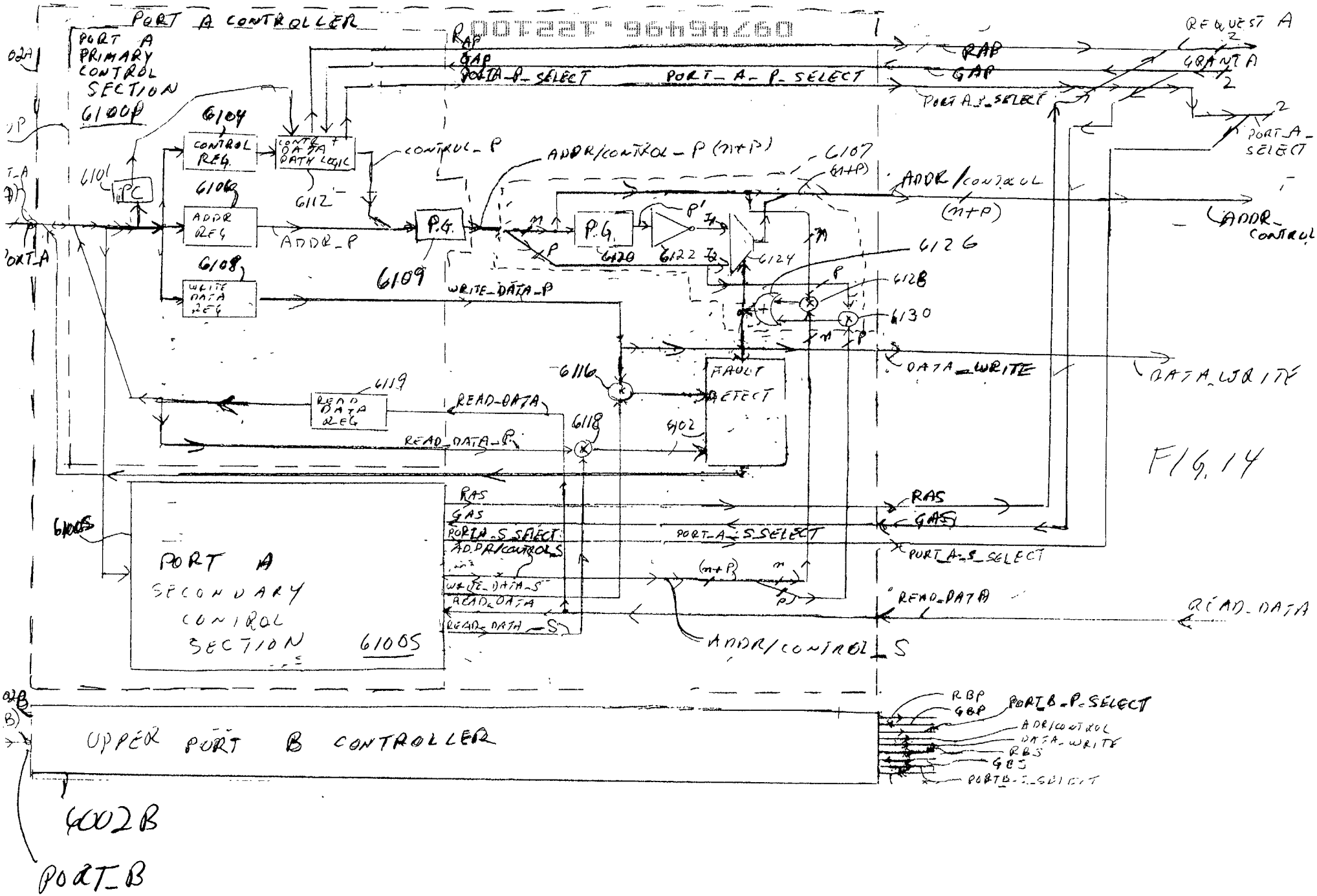
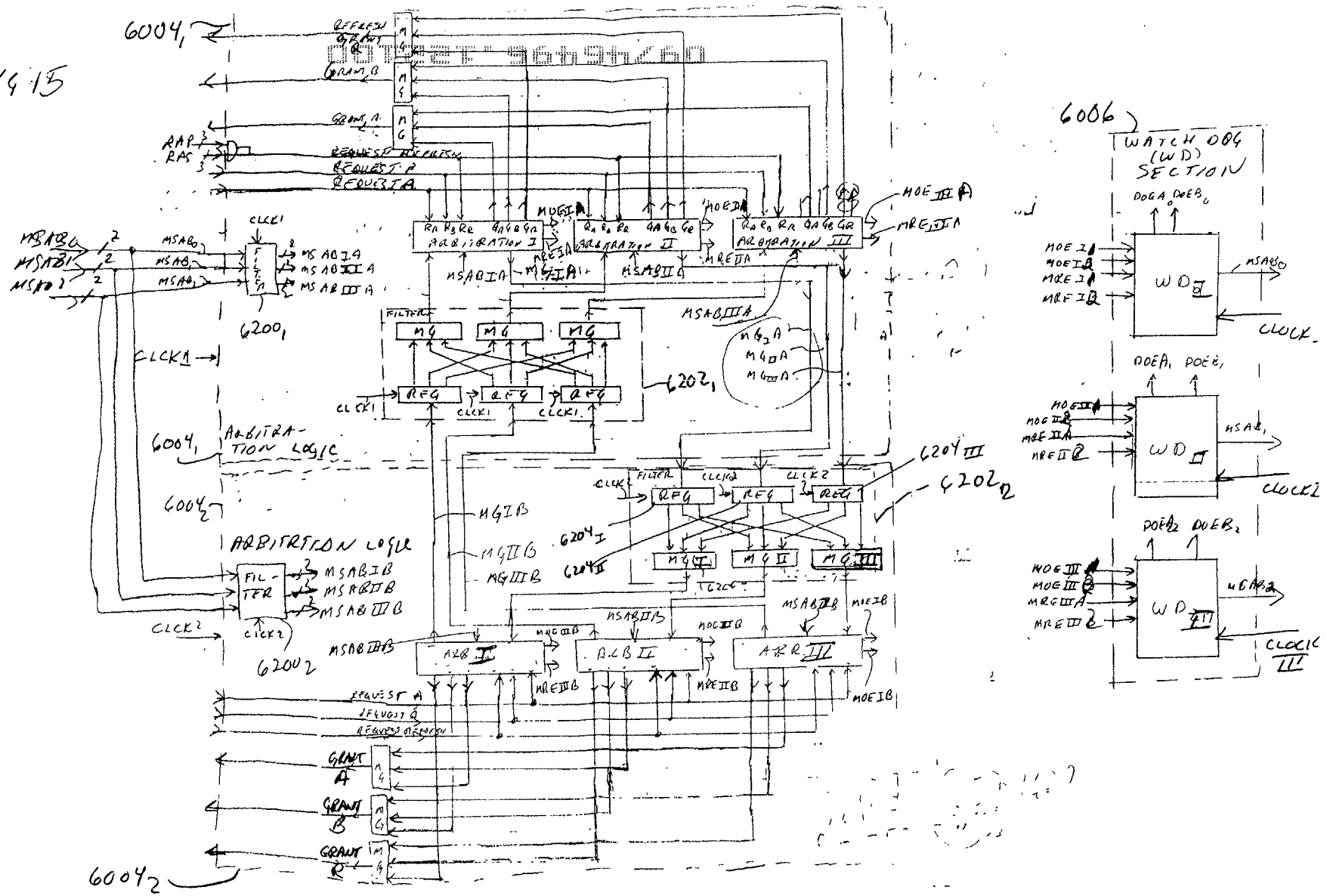

PORT A CONTROLLER
PORT A PRIMARY CONTROL SECTION 6100P
6104
CONTROL REG.
CONTROL DATA LOGIC
6112
CONTROL_P
6101
PC
6106
ADDR REG
ADDR_P
6108
WRITE DATA REG
6109
P.G.
ADDR/CONTROL_P (n+P)
6107
(n+P)
P.G.
6120
6122
6124
6126
6128
6130
WRITE_DATA_P
6116
FAULT DETECT
6102
6119
READ DATA REG
READ_DATA
READ_DATA_P
6118
RAS
GAS
PORT_A_S_SELECT
ADDR/CONTROL_S
WRITE_DATA_S
READ_DATA
READ_DATA_S
PORT A SECONDARY CONTROL SECTION 6100S
RAP
GAP
PORT_A_P_SELECT
REQUEST A
GRANT A
PORT_A_SELECT
ADDR/CONTROL (n+P)
ADDR_CONTROL
DATA_WRITE
READ_DATA
ADDR/CONTROL_S
RBP
GBP
PORT_B_P_SELECT
ADDR/CONTROL
DATA_WRITE
RBS
GBS
PORT_B_S_SELECT
UPPER PORT B CONTROLLER
6002B
PORT_B

FIG. 14

FIG 15


6004₁
6004₂
6200₁
6200₂
6204 I
6204 II
6204 III
6202₁
6202₂
6006
ARBITRATION LOGIC
ARBITRATION I
ARBITRATION II
ARBITRATION III
FILTER
REG
MG
WATCH DOG (WD) SECTION
WD I
WD II
WD III
CLOCK
CLOCK1
CLOCK2

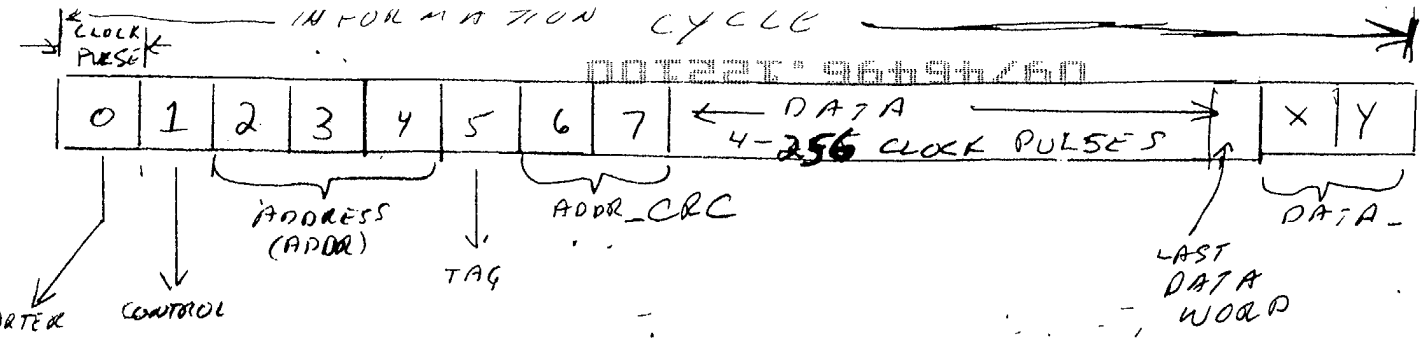


FIG. 16

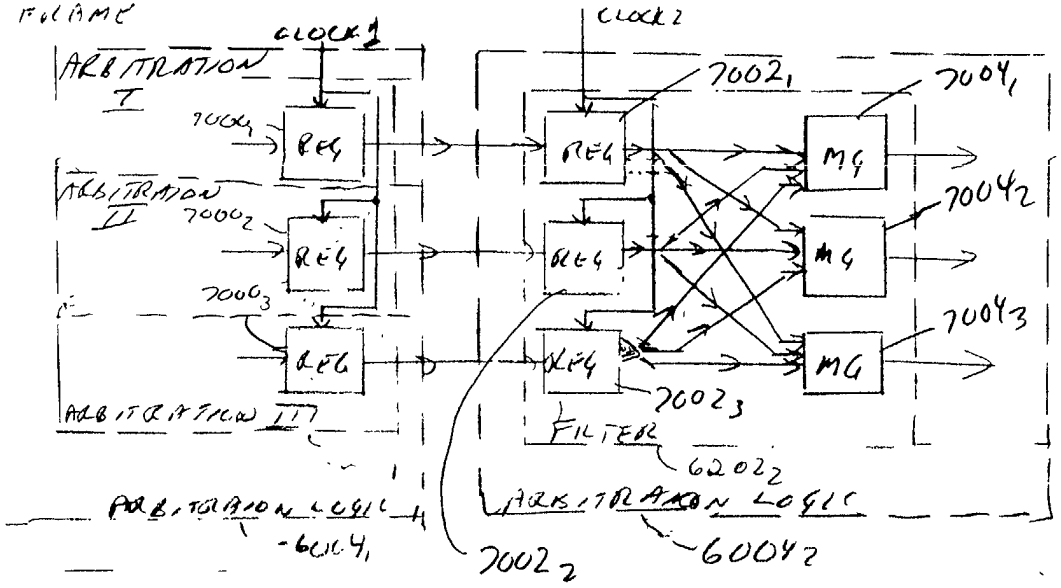


FIG. 18

FIG. 17

MG INPUTS	MG OUTPUT	MG OUTPUT	MG OUTPUT
0 0 0	0	0	0
0 0 1	0	0	0
0 1 0	0	0	0
0 1 1	1	1	1
1 0 0	0	0	0
1 0 1	1	1	1
1 1 0	1	1	1
1 1 1	1	1	1

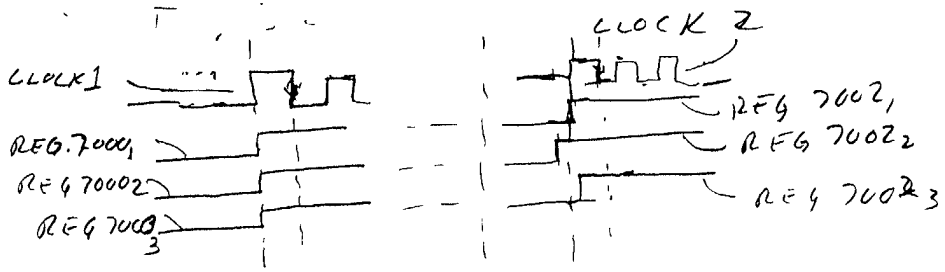
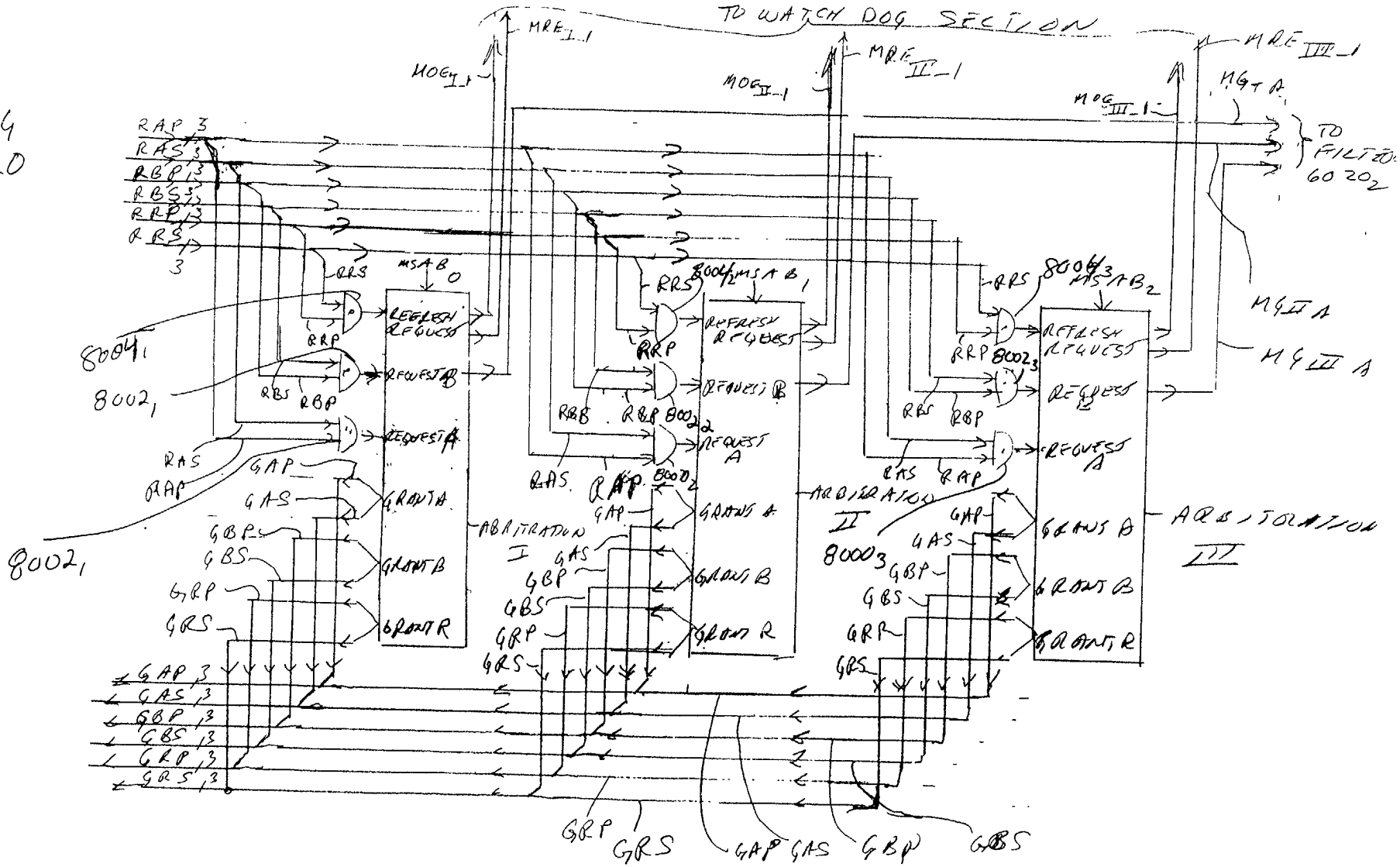


FIG. 19


TO WATCH DOG SECTION
MRE I_1
MRE II_1
MRE III_1
MOG I_1
MOG II_1
MOG III_1
MGT A
TO FILTER 60 20 2
MG II A
MG III A
RAP 3
RAS 3
RBP 3
RBS 3
RRP 3
RRS 3
MSAB 0
MSAB 1
MSAB 2
LEGLESH REQUEST
REFRESH REQUEST
REQUEST B
REQUEST A
GRANT A
GRANT B
GRANT R
ARBITRATION I
ARBITRATION II
ARBITRATION III
8004 1
8002 1
8002 2
8002 3
GAP
GAS
GBP
GBS
GRP
GRS
GAP 3
GAS 3
GBP 3
GBS 3
GRP 3
GRS 3

F64
20